

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
24 April 2003 (24.04.2003)

PCT

(10) International Publication Number
WO 03/034381 A2

(51) International Patent Classification⁷: **G09G**

[JP/JP]; c/o Corporate Research and Development Laboratory, Pioneer Corporation, 6-1-1, Fujimi, Tsurugashimashi, Saitama 350-2288 (JP).

(21) International Application Number: **PCT/JP02/09265**

(74) Agent: **FUJIMURA, Motohiko**; Fujimura & Associates, Ginza-Ohno Bldg., 1-17, Tsukiji 4-chome, Chuo-ku, Tokyo 104-0045 (JP).

(22) International Filing Date:
11 September 2002 (11.09.2002)

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(25) Filing Language: English

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),

(26) Publication Language: English

(30) Priority Data:
2001-286064 20 September 2001 (20.09.2001) JP

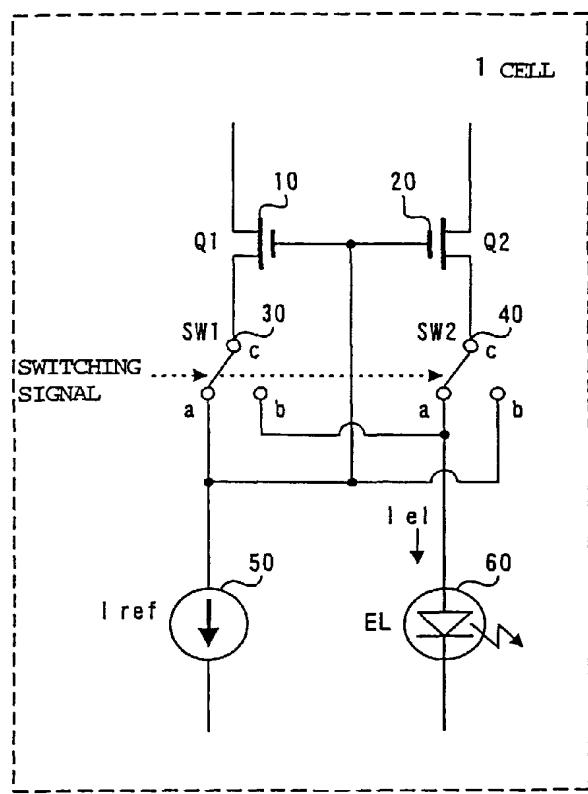
(71) Applicant (for all designated States except US): **PIioneer CORPORATION [JP/JP]**; 4-1, Meguro 1-chome, Meguro-ku, Tokyo 153-8654 (JP).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **OKUDA, Yoshiyuki**

[Continued on next page]

(54) Title: DRIVE CIRCUIT FOR LIGHT EMITTING ELEMENTS



(57) Abstract: ABSTRACT OF THE DISCLOSURE A display panel includes a number of light emitting cells arranged in a matrix. At least one drive circuit is associated with the light emitting cells. Each cell includes one light emitting element. A current mirror circuit is used in the drive circuit. The current mirror circuit has a primary transistor to drive a reference current source and a secondary transistor to drive the light emitting element. A pulse signal selects one of the primary and secondary transistors alternately. This switching operation by the pulse signal reduces irregularities in mirror ratio between the two transistors in each light emitting cell. As a result, the drive circuit(s) can suppress fluctuations in brightness among the light emitting cells of the display panel.

WO 03/034381 A2



Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

- *without international search report and to be republished upon receipt of that report*

DESCRIPTION

DRIVE CIRCUIT FOR LIGHT EMITTING ELEMENTS

Technical Field

This invention relates to a drive circuit for controlling the on/off state of light emitting elements arranged in a matrix on a display panel.

Background Art

Personal computers and data terminals have a display panel that includes a number of light emitting elements (or display cells) to display various types of information such as images and data. The light emitting elements are usually arranged in a matrix. Organic electroluminescent elements (referred to as "organic EL elements" hereinafter) are often used as the light emitting elements. The light emitting elements are generally driven by TFT (Thin Film Transistor) circuits. The TFT circuits can be formed together with the light emitting elements on the display panel.

A pair of neighboring transistors disposed on a general silicon semiconductor wafer have substantially the same characteristics. However, a low-temperature polysilicon TFT drive circuit, which is one of the most common drive circuits for the organic EL elements, has a drawback in that transistors formed on the drive circuit tend to have large irregularities in electric characteristics. In the TFT circuit, therefore, even the neighboring transistors might be very different in mutual inductance (so-called V_g - I_d property). Thus, when the TFT drive circuits are used for

the organic EL elements of the display panel, drive currents for the respective organic EL elements are not the same. This deteriorates quality of images displayed.

In order to eliminate the irregularities among the
5 organic EL element drive currents, Japanese Patent Application Kokai Nos. 2001-147659 and 2001-85988, published May 29, 2001 and March 30, 2001 respectively, disclosed use of a current mirror circuit. Specifically, a current mirror circuit is used such that the drive current for an organic
10 EL element is replaced with a reference current. This circuitry is schematically illustrated in Figure 1 of the accompanying drawings.

In Figure 1, reference symbols Qa and Qb denote a pair of transistors on the TFT circuit. A drain terminal of each
15 transistor is coupled to a power source. A source terminal of the transistor Qa is connected to a reference current source Iref, and a source terminal of the transistor Qb is connected to an organic EL element. The organic EL element is a load. A gate terminal of the transistor Qa is connected to a gate terminal of the transistor Qb. The gate terminal of the transistor Qa is also connected to the source terminal. In this manner, the transistors Qa and Qb form a current mirror circuit. A square of the broken line in Figure 1 indicates a single cell (or one pixel) in the
20 display panel. In other words, Figure 1 shows a drive circuit structure for the single cell.
25

The drive circuit of Figure 1 operates as follows. The

following equation holds true because of a mirror image current effect in the current mirror circuit when drain currents of the transistors Qa and Qb are represented by symbols I_{da} and I_{db} :

5

$$I_{da} \doteq I_{db}$$

The drain current of each transistor is substantially the same as the source current. The source current for the 10 transistor Qa is the reference current I_{ref} , and the source current for the transistor Qb is a drive current I_{el} of the organic EL element. Therefore, the following equations are established:

15

$$I_{da} \doteq I_{ref}$$

$$I_{db} \doteq I_{el}$$

From the above described equations, the following equation results:

20

$$I_{ref} \doteq I_{el}$$

Therefore, the drive current I_{el} for the organic EL element in the single cell is not influenced by the 25 characteristics of the transistors Qa and Qb situated in the drive circuit, but determined by the value of the reference current source I_{ref} only.

In the drive circuit shown in Figure 1, the organic EL element drive current I_{el} becomes equal to the predetermined reference current I_{ref} in each of the cells of the display panel. As a result, it is possible to suppress 5 irregularities, among the cells in emission brightness, to a certain extent.

However, when a low-temperature polysilicon TFT circuit is used, great irregularities appear in characteristics between the neighboring transistors so that the two 10 transistors Q_a and Q_b of the current mirror circuit shown in Figure 1 do not have the same electrical characteristics. Accordingly, a mirror ratio, M_r , which represents a ratio of a secondary current (current flowing in the secondary transistor Q_b) to a primary current (current flowing in the 15 primary transistor Q_a) in the current mirror circuit does not become 1. Ideally, the mirror ratio M_r (= secondary current/primary current) should be 1.

Therefore, even if the primary current, i.e., the reference current I_{ref} , is stable in the current mirror 20 circuit, the secondary current, i.e., the organic EL element drive current I_{el} , becomes:

$$I_{el} = I_{ref} \times M_r \neq I_{ref}$$

Consequently, the organic EL element drive currents are 25 not the same among the cells of the display panel. Thus, the cells do not emit light at uniform brightness, and

unfavorable patterns appear in the display screen. The display screen having such patterns is sometimes referred to as a "sand-spreading screen."

Disclosure of Invention

5 An object of the present invention is to provide a drive circuit for a light emitting element that can reduce fluctuations in brightness among light emitting cells of a display panel.

According to one aspect of the present invention, there
10 is provided a drive circuit for driving a light emitting element with a current having a predetermined value, comprising: a current mirror circuit including a primary transistor and a secondary transistor; a reference current source for providing the current having the predetermined current value; a switching element for alternately connecting the primary transistor to one of the light emitting element and the reference current source and for alternately connecting the secondary transistor to the other of the light emitting element and the reference current source; and a switchover controller for controlling the switching element to connect the primary transistor to the light emitting element when the secondary transistor is connected to the reference current source, and to connect the primary transistor to the reference current source when the secondary transistor is connected to the light emitting element.

A display panel includes a number of light emitting

elements and cells arranged in a matrix. One drive circuit is associated with one light emitting cell. Since the driving circuits can provide uniform drive currents in the respective light emitting cells, it is possible to reduce 5 the fluctuations in brightness among the pixels (cells) and improve the quality of images displayed on the screen.

Brief Description of Drawings

Figure 1 illustrates a circuit diagram of a drive circuit for an organic EL element which uses a current 10 mirror circuitry;

Figure 2 is a circuit diagram showing a drive circuit for an organic EL element in accordance with a first embodiment of the present invention;

Figure 3 depicts relationship between a mirror ratio 15 variation and a mirror ratio deviation;

Figure 4 illustrates a drive circuit similar to Figure 2, but has a TFT structure;

Figure 5 illustrates a drive circuit for an organic EL element in accordance with a second embodiment of the 20 present invention;

Figure 6 illustrates a drive circuit similar to Figure 5, but has a TFT structure;

Figure 7 illustrates a drive circuit for an organic EL element in accordance with a third embodiment of the present 25 invention; and

Figure 8 illustrates a drive circuit similar to Figure 7, but has a TFT structure.

Detailed Description of the Invention

Embodiments of the present invention will be described with reference to Figures 2 to 8.

Referring first to Figure 2, a first embodiment of a drive circuit for an organic EL element according to the present invention is illustrated.

The circuit configuration of the first embodiment will be first described. In Figure 2, each of elements Q1 (10) and Q2 (20) functions as a TFT transistor element. The TFT transistor element may be a bipolar transistor or FET (Field Effect Transistor). Any element serving as a transistor is called "transistor" in the following description.

Drain terminals of the transistors Q1 (10) and Q2 (20) are coupled to power sources respectively. Gate terminals of the transistors Q1 (10) and Q2 (20) are connected to each other, and to source terminals via switching elements SW1 and SW2 respectively. Therefore, the transistors Q1 (10) and Q2 (20) form a current mirror circuit, and a current substantially equal to a drain current in the primary transistor Q1 (10) is caused to always flow in the secondary transistor Q2 (20) as a drain current.

A switching element SW1 (30) and a switching element SW2 (40) are TFT switching elements. Like the transistor Q1 (or Q2), each switching element SW1 (or SW2) may be a bipolar transistor or FET. The switching elements SW1 (30) and SW2 (40) serve as alternate switching elements, which switch over simultaneously in accordance with a level of a

switching signal supplied from a source (not shown). Each switching element includes one common terminal (referred to as "terminal c") and two independent terminals "a" and "b". The terminal c is connected to the terminal a/b alternately 5 in accordance with the switching signal level. In this embodiment, the terminal c is coupled to the terminal a when the switching signal level is high, and the terminal c is coupled to the terminal b when the switching signal level is low.

10 The terminal c of the switching element SW1 (30) is connected to the source terminal of the transistor Q1 (10). The terminal c of the switching element SW2 (40) is connected to the source terminal of the transistor Q2 (20). The terminal a of the switching element SW1 (30) and the 15 terminal b of the switching element SW2 (40) are connected to a reference current source (50), the gate terminal of the transistor Q1 (10) and the gate terminal of the transistor Q2 (20). The terminal b of the switching element SW1 (30) and the terminal a of the switching element SW2 (40) are 20 connected to an organic EL element (60).

 The switching operation of the switching element SW1 between the terminal a (reference current source) and the terminal b (organic EL element) takes place preferably at high speed. Likewise, the switching operation of the 25 switching element SW2 between the terminal a (organic EL element) and the terminal b (reference current source) takes place at high speed. The switching operation of the

switching element SW1 takes place in synchronization with the switching operation of the switching element SW2.

The reference current source (50) is a constant current circuit, comprising a TFT transistor element, to supply a 5 constant current I_{ref} regardless of a value of voltage applied to the reference current source.

The organic EL element (60) is a light emitting element using organic electroluminescent materials, and emits light when the predetermined drive current I_{el} flows.

10 Now the operation of the circuit shown in Figure 2 will be described.

It should be noted that a display panel includes a number of cells, each cell includes a light emitting element (organic EL element), and at least one of the light emitting 15 elements is selected for light emission. A selection signal supplied to the display panel selects the light emitting element(s).

In this embodiment, a switching signal for the switching elements SW1 (30) and SW2 (40) is a pulse signal 20 having high and low levels alternately. For example, the high level of the pulse signal alternates with the low level for each frame of the display screen or each sub-frame.

It should be assumed that the high level of the pulse signal is first applied to the switching elements SW1 (30) 25 and SW2 (40). As described earlier, the terminal c of the switching element SW1 (30) is connected to the terminal a when the switching signal is at the high level. At the same

time, the terminal c of the switching element SW2 (40) is connected to the terminal a. Therefore, the source terminal of the transistor Q1 (10) is coupled to the reference current source (50), and the source terminal of the 5 transistor Q2 (20) is coupled to the organic EL element (60).

As a result, a gate-source voltage appears at the transistor Q1 (10) such that the drain current in the transistor Q1 (10) becomes the current I_{ref} of the reference current value (50). Since the gate terminal of the 10 transistor Q1 is connected to the gate terminal of the transistor Q2, the gate-source voltage is also applied to the transistor Q2. A drain current which corresponds to the gate-source voltage is therefore caused to flow in the transistor Q2. The drain currents of the transistors Q1 and 15 Q2 at this moment are represented by I_{d1} and I_{d2} . Deviation of the mirror ratio of the current mirror circuit that includes the transistors Q1 and Q2 is represented by x ($0 \leq |x| \ll 1$). Then, the following equation is established:

$$20 \quad I_{d1} : I_{d2} = 1 : (1 + x) \quad (1)$$

Therefore, the difference between the drain currents I_{d1} and I_{d2} decreases as the absolute value of the mirror ratio deviation x decreases. If the characteristics of the 25 two transistors Q1 and Q2 in the current mirror circuit are the same, the mirror ratio deviation x is zero, i.e., $I_{d1} = I_{d2}$.

As described above, the drain current is substantially equal to the source current in each of the primary and secondary transistors in the current mirror circuit. Therefore, by substituting the source currents I_{ref} and I_{el} for the transistor drain currents I_{d1} and I_{d2} respectively, 5 the equation (1) is expressed as follows:

$$I_{el} = I_{ref} \times (1 + x) \quad (2)$$

10 It should be assumed now that the switching pulse signal applied to the switching elements SW1 and SW2 changes from the high level to the low level.

On this occasion, the terminal c of the switching element SW1 is switched over to the terminal b from the 15 terminal a, and the terminal c of the switching element SW2 is switched over to the terminal b from the terminal a. Specifically, the source terminal of the transistor Q1 (10) is connected to the organic EL element 60 and the source terminal of the transistor Q2 (20) is connected to the 20 reference current source 50. Then, a gate-source voltage appears at the transistor Q2 and the drain current becomes I_{ref} . This gate-source voltage is also applied to the transistor Q1, and a corresponding drain current is generated in the transistor Q1.

25 Consequently, the following equation is established between the drive current I_{el} in the organic EL element 60 and the reference current I_{ref} of the reference current

source 50:

$$I_{el} = I_{ref} / (1 + x) \quad (3)$$

5 This equation is obtained in a similar manner as the equations (1) and (2) are obtained.

The switching signal applied to the switching elements SW1 and SW2 is the pulse signal having the alternating high and low levels for each frame of the display screen or each 10 sub-frame, as mentioned above. If a duty factor of the pulse waveform is 1/2, then the high level has the same period (time length) as the low level.

An average value of the organic EL element drive current I_{el} per unit time is represented by $I_{el(AV)}$ in this 15 embodiment. $I_{el(AV)}$ is then given by the average of the sum of the equations (2) and (3), and the following equation (4) is established:

$$\begin{aligned} I_{el(AV)} &= I_{ref} \times \{(1 + x) + 1 / (1 + x)\} / 2 \\ 20 &= I_{ref} \times \{1 + x^2/2 \times (1 + x)\} \end{aligned} \quad (4)$$

The mirror ratio deviation x in the equations (2) and (4) can be expressed by the mirror ratio Mr (or $Mr(AV)$) in the following manner. In other words, the mirror Mr (or 25 $Mr(AV)$) can be expressed by the mirror ratio deviation x as described below.

As mentioned above, the mirror ratio Mr (or $Mr(AV)$) is

a ratio of the secondary current I_{el} (or its average $I_{el(AV)}$) of the current mirror circuit to the primary current I_{ref} . The mirror ratio deviation x indicates deviation of an actual mirror ratio from the theoretical value (one).

Therefore, the mirror ratio Mr in the equation (2) can be expressed as follows:

$$\begin{aligned} I_{el} &= I_{ref} \times Mr \\ 10 \quad \therefore Mr &= 1 + x \end{aligned}$$

The mirror ratio Mr of this equation is the mirror ratio of the current mirror circuit in the drive circuit shown in Figure 1.

15 On the other hand, the mirror ratio $Mr(AV)$ in the equation (4), which represents the embodiment of the invention, can be expressed as follows:

$$\begin{aligned} I_{el(AV)} &= I_{ref} \times Mr(AV) \\ 20 \quad \therefore Mr(AV) &= 1 + x^2/2 \times (1 + x) \end{aligned}$$

Figure 3 depicts the mirror ratios Mr and $Mr(AV)$ with respect to the mirror ratio deviation x , which are calculated by the above equations. It is clear from the characteristic curves of Figure 3 that the mirror ratio $Mr(AV)$ fluctuates significantly less than the mirror ratio Mr .

Therefore, even if the two neighboring transistors (a pair of transistors) in the current mirror circuit using the low-temperature polysilicon TFT have different characteristics and have a large mirror ratio deviation x ,

5 it is possible to suppress the mirror ratio variations, which is caused by the mirror ratio deviation, within a very small range by employing the circuitry shown in Figure 2. In other words, even if the two transistors have different characteristics, the drive current I_{el} of the organic EL

10 element is very close to the current value I_{ref} of the reference current source. Accordingly, the brightness of the organic EL elements arranged in a matrix on the display panel becomes uniform, and no "sand-spreading" pattern appears on the display screen.

15 Referring to Figure 4, an example of a TFT circuit designed on the basis of the circuit of Figure 2 is illustrated. The transistors Q31 and Q32 and an inverting circuit (INV) of Figure 4 correspond to the switching element SW1 of Figure 2. The transistors Q41 and Q42 and

20 the inverting circuit (INV) of Figure 4 correspond to the switching element SW2 of Figure 2. Therefore, when the switching signal level is high, the transistors Q31 and Q41 are turned on and the transistors Q32 and Q42 are turned off. On the other hand, when the switching signal level is low,

25 the transistors Q32 and Q42 are turned on and the transistors Q31 and Q41 are turned off.

Other circuit elements, such as the transistors Q1 and

Q2, in Figure 4 will not be described here since they are similar to those illustrated in Figure 2.

A second embodiment of the present invention will be described with reference to Figure 5.

5 Similar reference numerals and symbols are used to designate similar elements in Figures 2 and 5, and these elements will not be described in detail.

10 In the organic EL element drive circuit according to the second embodiment, the transistors Q1 (10) and Q2 (20), the switching elements SW1 (30) and SW2 (40) and the organic EL element (60) are connected in a similar manner to the first embodiment.

15 One difference between the first and second embodiments lies in that a resistor element R1 (70) is used in the place of the reference current source (50). This is because a simple resistor is often substituted for a constant current source in an electronic circuit when a relatively small current flows in the electronic circuit. A typical example of such electronic circuit is a differential amplifier circuit. Another reason is because substituting the resistors for the reference current sources (50) is very practical, since the display panel includes a number of cells and each cell needs the reference current source (50).

20 It should be noted that a switching element SW3 (72) is explicitly illustrated in Figure 5. The switching element SW3 turns on and off the organic EL element in the display cell. The switching element SW3 is included in the circuit

of Figure 2, but not illustrated.

The switching element SW3 is controlled by an on/off signal (control signal) from a display control circuit (not shown). The display control circuit is connected to the 5 display panel. One end of the switching element SW3 is connected to the power source, and the other end is connected to the gate terminals of the transistors Q1 (10) and Q2 (20). The gate terminal of the transistor Q1 is connected to the gate terminal of the transistor Q2 (20).

10 In this embodiment, the primary and secondary transistors of the current mirror circuit are switched over by the switching elements at high speed, and the influence of the mirror ratio deviation is reduced in a similar manner to the first embodiment of Figure 2. Therefore, the 15 detailed description of the operation of the second embodiment in this regard is omitted.

Figure 6 illustrates an example of a TFT circuit, which is substantially equivalent to the circuit of Figure 5. The transistors Q31 and Q32 and an inverting circuit (INV) of 20 Figure 6 correspond to the switching element SW1 of Figure 5. The transistors Q41 and Q42 and the inverting circuit (INV) of Figure 6 correspond to the switching element SW2 of Figure 5. Therefore, when the switching signal level is high, the transistors Q31 and Q41 are turned on and the 25 transistors Q32 and Q42 are turned off. On the other hand, when the switching signal level is low, the transistors Q32 and Q42 are turned on and the transistors Q31 and Q41 are

turned off.

The transistor Q3 in Figure 6 corresponds to the switching element SW3 (72) in Figure 5.

A third embodiment of the present invention will be 5 described with reference to Figure 7.

Similar reference numerals and symbols are used to designate similar elements in Figures 2 and 7, and these elements will not be described in detail.

In the organic EL element drive circuit according to 10 the third embodiment, the reference current source (50) is provided outside the cell such that a plurality of cells of the display panel share the reference current source (50). The reference current source (50) should be highly precise and requires a complicated circuit structure. By sharing 15 one current source (50) with a plurality of cells, it is possible to reduce the total number of the current sources in the display panel. The on/off control of each cell for light emission/extinction is made by controlling the reference current source (50). Accordingly, the switching 20 element SW3 (72) in Figure 5 is dispensed with.

It should be noted, however, that the reference current Iref is supplied to a target cell from the reference current source (50) only when a line selection signal from an image display control unit (not shown) specifies the target cell 25 by line addressing, since the reference current source (50) is shared by a plurality of cells. Therefore, a voltage holding element should be provided for holding an electrical

charge carried by the reference current when the target cell is selected and the reference current I_{ref} is fed to the target cell. This voltage holding element also holds a voltage derived from the electrical charge of the reference current to use the voltage as a gate voltage of the transistor of the current mirror circuit. Further, a switchover element should be provided for connecting the voltage holding element to the reference current source (50) when the target cell is specified by line addressing, and for disconnecting the voltage holding element from the reference current source (50) when another cell is specified by line addressing.

In this embodiment, a capacitor C1 (80) serves as the voltage holding element, and switching elements SW4 (82) and SW5 (84) serve as the switchover element.

Specifically, the line selection signal is applied to the control terminals of the switching elements SW4 and SW5 from the external image display control unit (not shown) such that the on/off control of the switching elements SW4 and SW5 is conducted by the line selection signal. One end of the switching element SW5 (84) is coupled with the reference current source (50), and the other end of the switching element SW5 is coupled with the terminal a of the switching element SW1 (30), the terminal b of the switching element SW2 (40) and one end of the switching element SW4 (82). The other end of the switching element SW4 (82) is coupled with one end of the capacitor C1 (80), the gate

terminal of the transistor Q1 (10) and the gate terminal of the transistor Q2 (20). The other end of the capacitor C1 (80) is coupled with the power source.

Other elements and structure of the drive circuit of 5 this embodiment are similar to those of the first and second embodiments. The operation principle of these elements is also the same as the first and second embodiments. Therefore, the description thereof is omitted.

Figure 8 shows a TFT circuit configured on the basis of 10 the circuit of Figure 7. The transistors Q31 and Q32 and an inverting circuit (INV) of Figure 8 correspond to the switching element SW1 of Figure 7. The transistors Q41 and Q42 and the inverting circuit (INV) of Figure 8 correspond to the switching element SW2 of Figure 7. Therefore, when 15 the switching signal level is high, the transistors Q31 and Q41 are turned on and the transistors Q32 and Q42 are turned off. On the other hand, when the switching signal level is low, the transistors Q32 and Q42 are turned on and the transistors Q31 and Q41 are turned off. The transistors Q4 20 and Q5 in Figure 8 correspond to the switching elements SW4 and SW5 in Figure 7.

The organic EL element is utilized as a light emitting element to be driven by the drive circuit in the foregoing embodiments. However, the light emitting element is not limited to an organic EL element. For instance, inorganic EL light emitting elements and light emitting diodes may be used. Liquid crystal display elements are also employable.

This application is based on a Japanese patent application No. 2001-286064 and the entire disclosure thereof is incorporated herein by reference.

CLAIMS

1. A drive circuit for driving a light emitting element with a current having a predetermined value, comprising:

5 a current mirror circuit including a primary transistor and a secondary transistor;

a reference current source for providing the current having the predetermined value;

10 a switching element for alternately connecting the primary transistor to one of the light emitting element and the reference current source and for alternately connecting the secondary transistor to the other of the light emitting element and the reference current source; and

15 a switchover controller for controlling the switching element to connect the primary transistor to the light emitting element when the secondary transistor is connected to the reference current source, and to connect the primary transistor to the reference current source when the secondary transistor is connected to the light emitting 20 element.

2. The drive circuit according to claim 1 further including a second switching element for on/off control of the current mirror circuit on the basis of a control signal which provides on/off control of the light emitting element.

25 3. The drive circuit according to claim 1, wherein the reference current source is a resistor.

4. The drive circuit according to claim 1, wherein the

switchover controller controls the switching element in response to a predetermined external signal.

5. The drive circuit according to claim 4, wherein the predetermined external signal is a synchronization signal included in an audiovisual signal supplied to the drive circuit.

6. The drive circuit according to claim 4, wherein the predetermined external signal is a signal in synchronization with a sub-frame, the sub-frame being obtained by dividing 10 an audiovisual signal into a plurality of sub-frames.

7. The drive circuit according to claim 1, wherein said light emitting element is one of an organic electroluminescent light emitting element, an inorganic electroluminescent light emitting element, a light emitting diode, and a liquid crystal display element. 15

8. The drive circuit according to claim 1, wherein said primary transistor is one of a bipolar transistor and an FET.

9. The drive circuit according to claim 1, wherein the 20 switchover controller permits high speed alternate switching between the light emitting element and the reference current source.

10. An arrangement for driving a plurality of light emitting elements with a current having a predetermined 25 value, comprising:

a reference current source for providing the current having the predetermined value, the reference current source

being shared by the plurality of light emitting elements;
a plurality of drive circuits associated with the plurality of light emitting elements respectively;
each drive circuit including:
5 a current mirror circuit having a primary transistor and a secondary transistor,
a first switching element for alternately connecting the primary transistor of the current mirror circuit to one of the light emitting element and the reference current source and for alternately connecting the secondary transistor to the other of the light emitting element and the reference current source,
10
15 a switchover controller for controlling the first switching element to connect the primary transistor of the current mirror circuit to the light emitting element when the secondary transistor is connected to the reference current source, and to connect the primary transistor to the reference current source when the secondary transistor is connected to the light emitting element,
20
25 an electrical charge holding element for holding an electrical charge supplied from the reference current source, and applying a voltage corresponding to the electrical

charge to a gate of each of the primary and secondary transistors of the current mirror circuit, and

5 a second switching element for connecting and disconnecting the electrical charge holding element to the reference current source based on a signal selecting the drive circuit.

11. The drive circuit according to claim 10, wherein each switchover controller controls the first switching 10 element in response to a predetermined external signal.

12. The drive circuit according to claim 11, wherein the predetermined external signal is a synchronization signal included in an audiovisual signal supplied to the drive circuit.

15 13. The drive circuit according to claim 11, wherein the predetermined external signal is a signal in synchronization with a sub-frame, the sub-frame being obtained by dividing an audiovisual signal into a plurality of sub-frames.

20 14. The drive circuit according to claim 10, wherein said light emitting element is one of an organic electroluminescent light emitting element, an inorganic electroluminescent light emitting element, a light emitting diode, and a liquid crystal display element.

25 15. The drive circuit according to claim 10, wherein the reference current source is a resistor.

16. The drive circuit according to claim 10, wherein

said primary transistor is one of bipolar transistor and an FET.

17. The drive circuit according to claim 10, wherein the switchover controller provides high speed alternate switching between the light emitting element and the reference current source.

18. A display cell for a display panel, comprising:
a current mirror circuit including a primary transistor and a secondary transistor;

10 a light emitting element, which emits light in response to a predetermined current;

a switching element for alternately connecting the primary transistor to one of the light emitting element and a reference current source and for alternately connecting 15 the secondary transistor to the other of the light emitting element and the reference current source; and

a switchover controller for controlling the switching element to connect the primary transistor to the light emitting element when the secondary transistor is connected 20 to the reference current source, and to connect the primary transistor to the reference current source when the secondary transistor is connected to the light emitting element.

19. The display cell according to claim 18 further 25 including a reference current source for providing the predetermined current.

20. The display cell according to claim 18, wherein the switchover controller provides high speed alternate switching between the light emitting element and the reference current source.

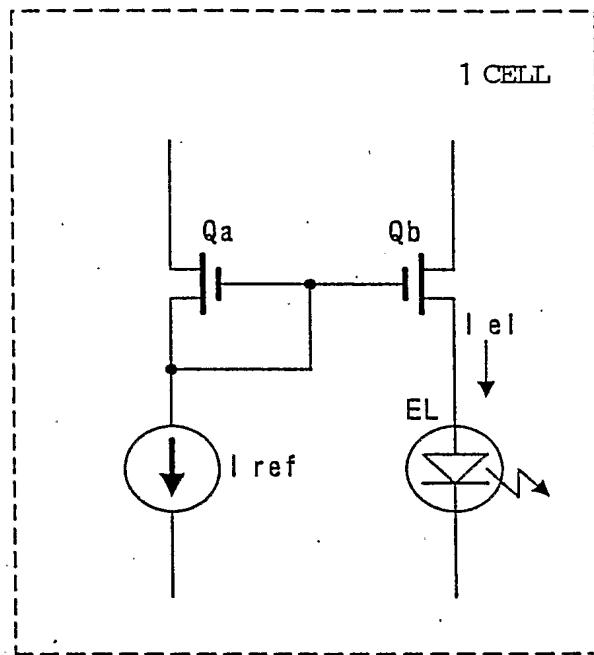


FIG. 1

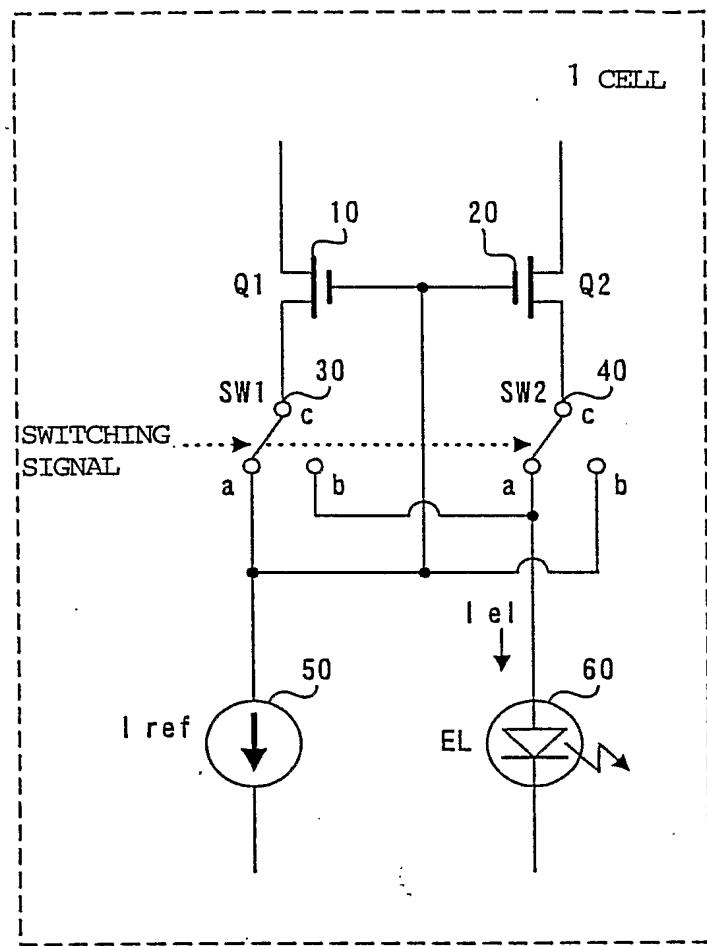


FIG. 2

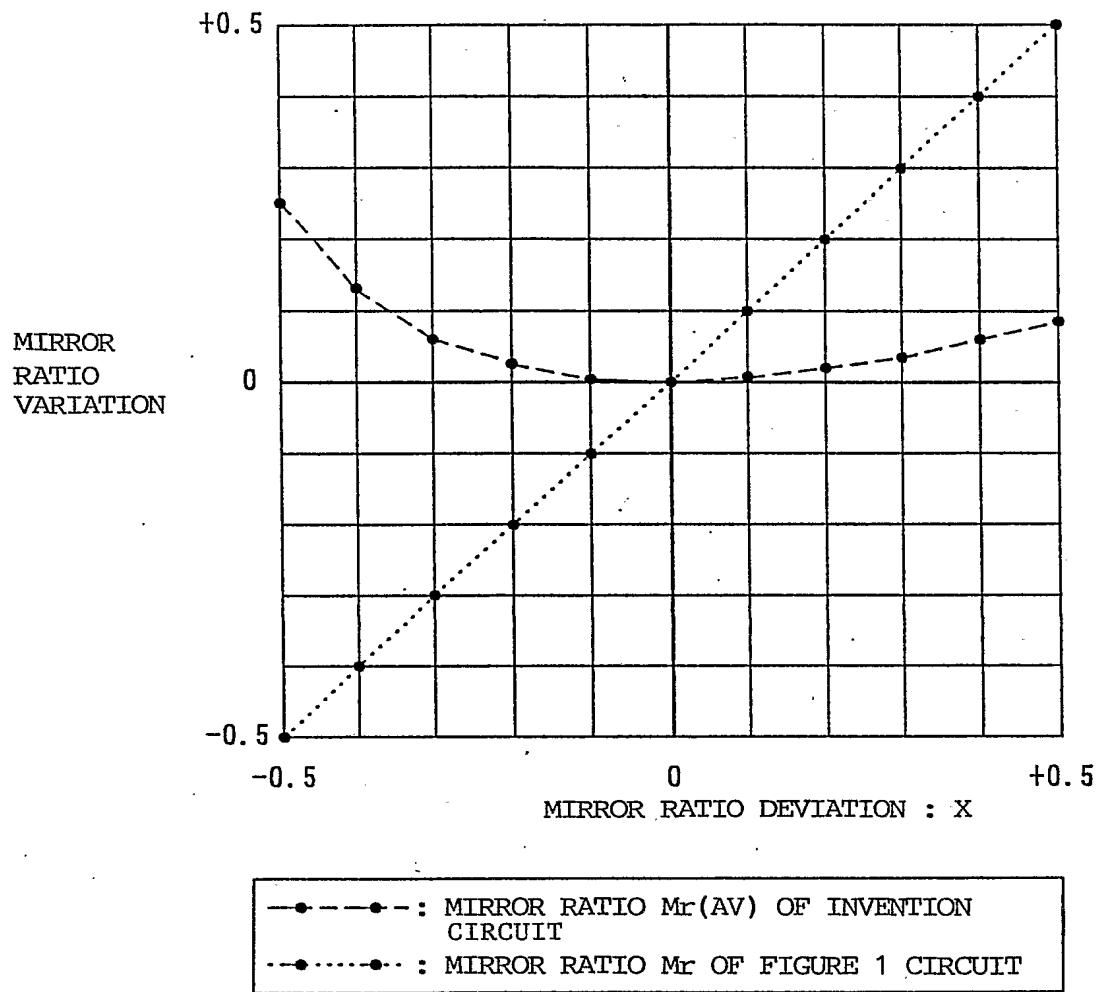
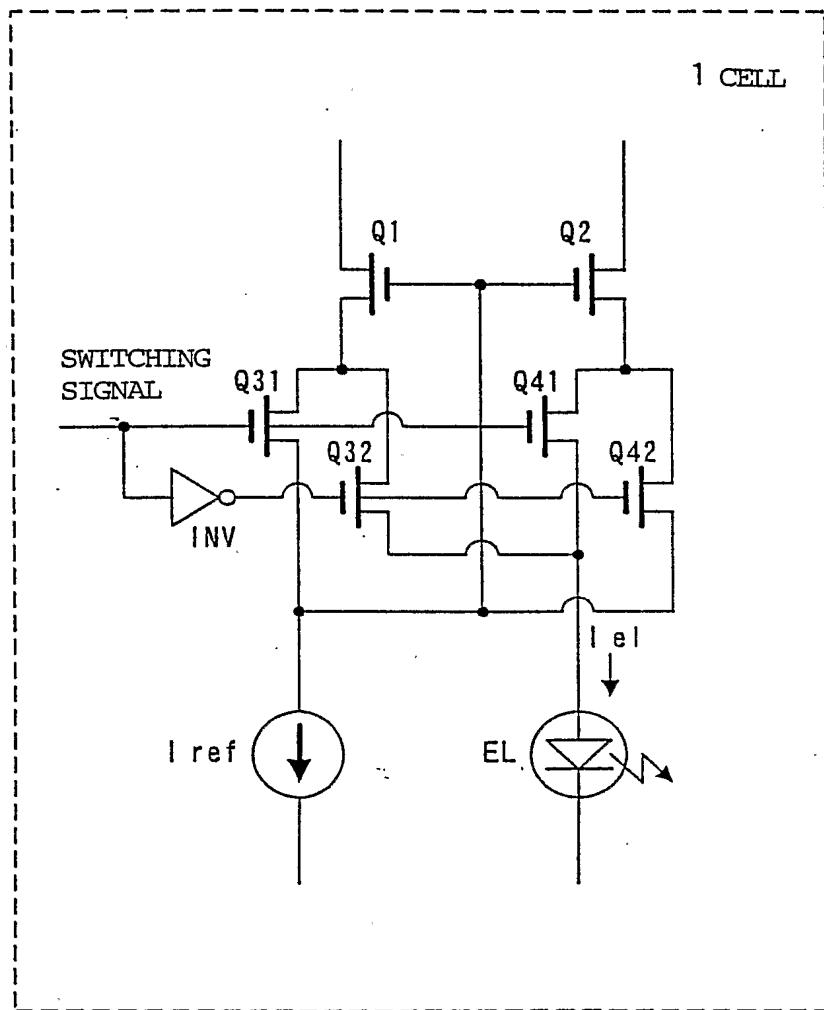


FIG. 3



F I G . 4

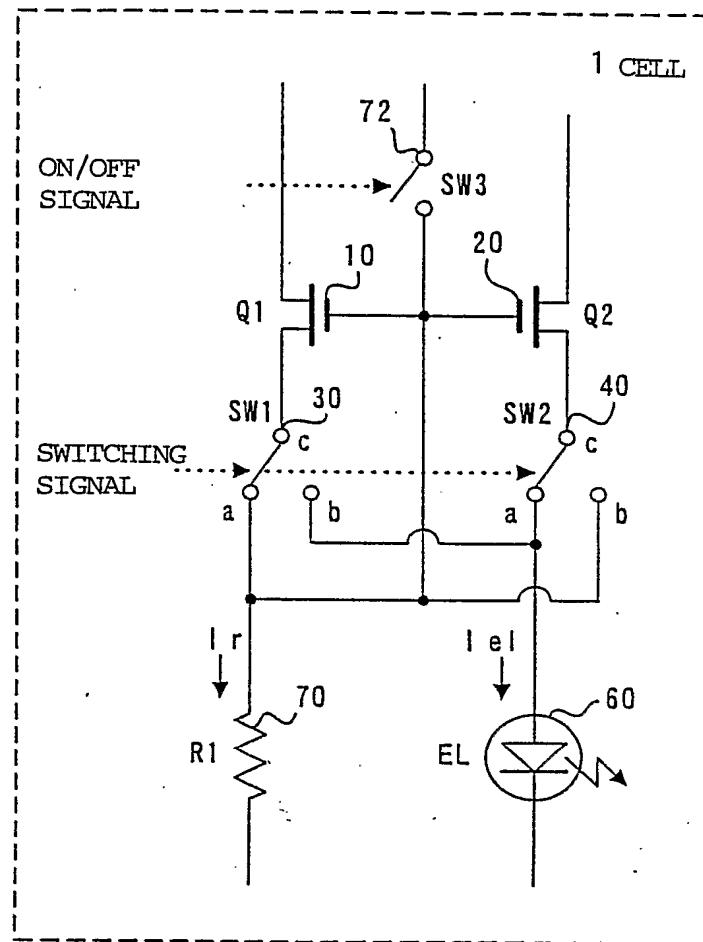


FIG. 5

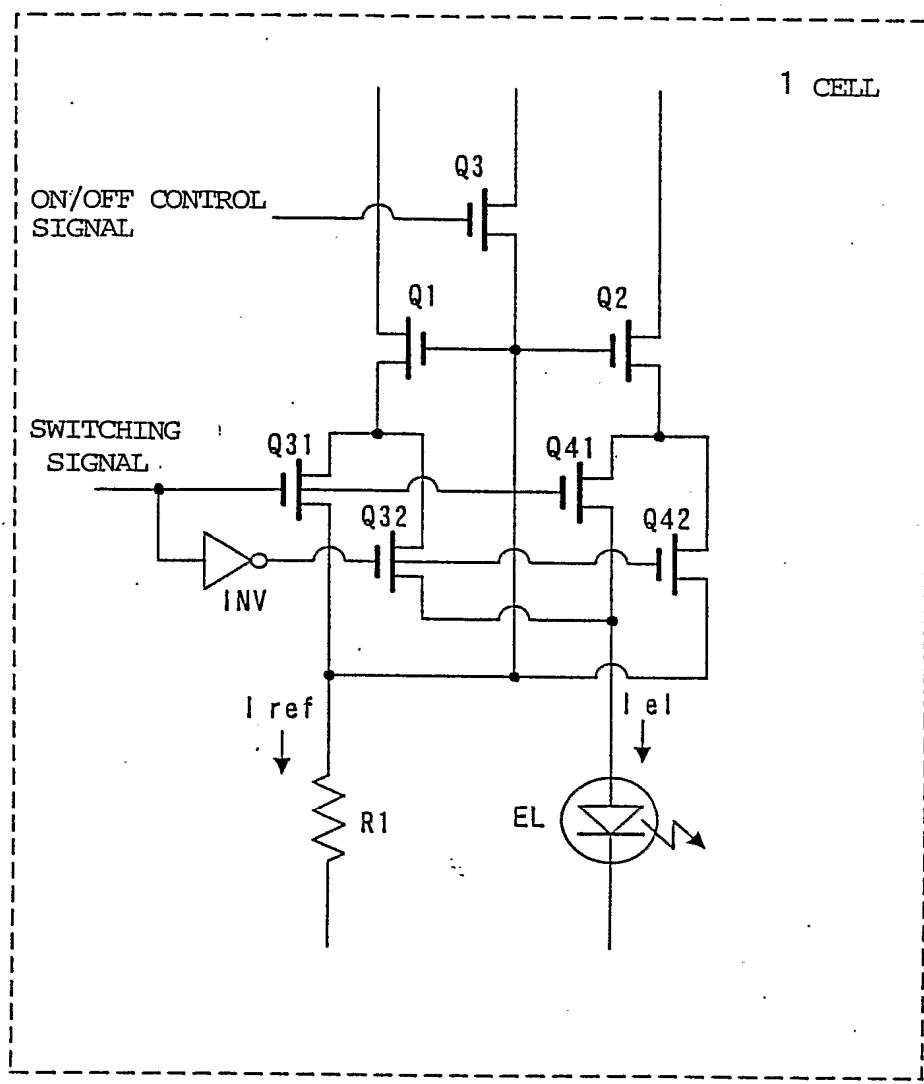


FIG. 6

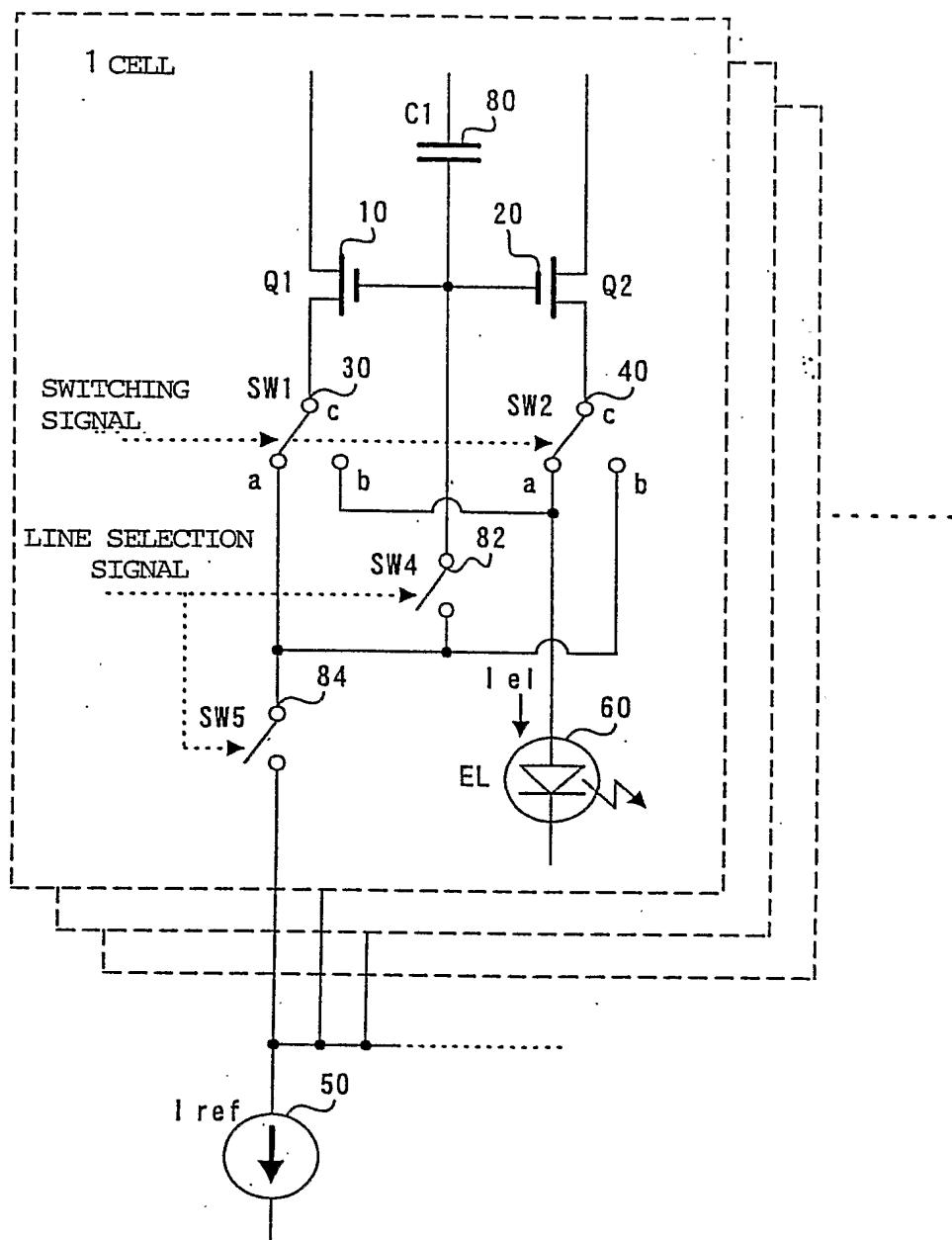


FIG. 7

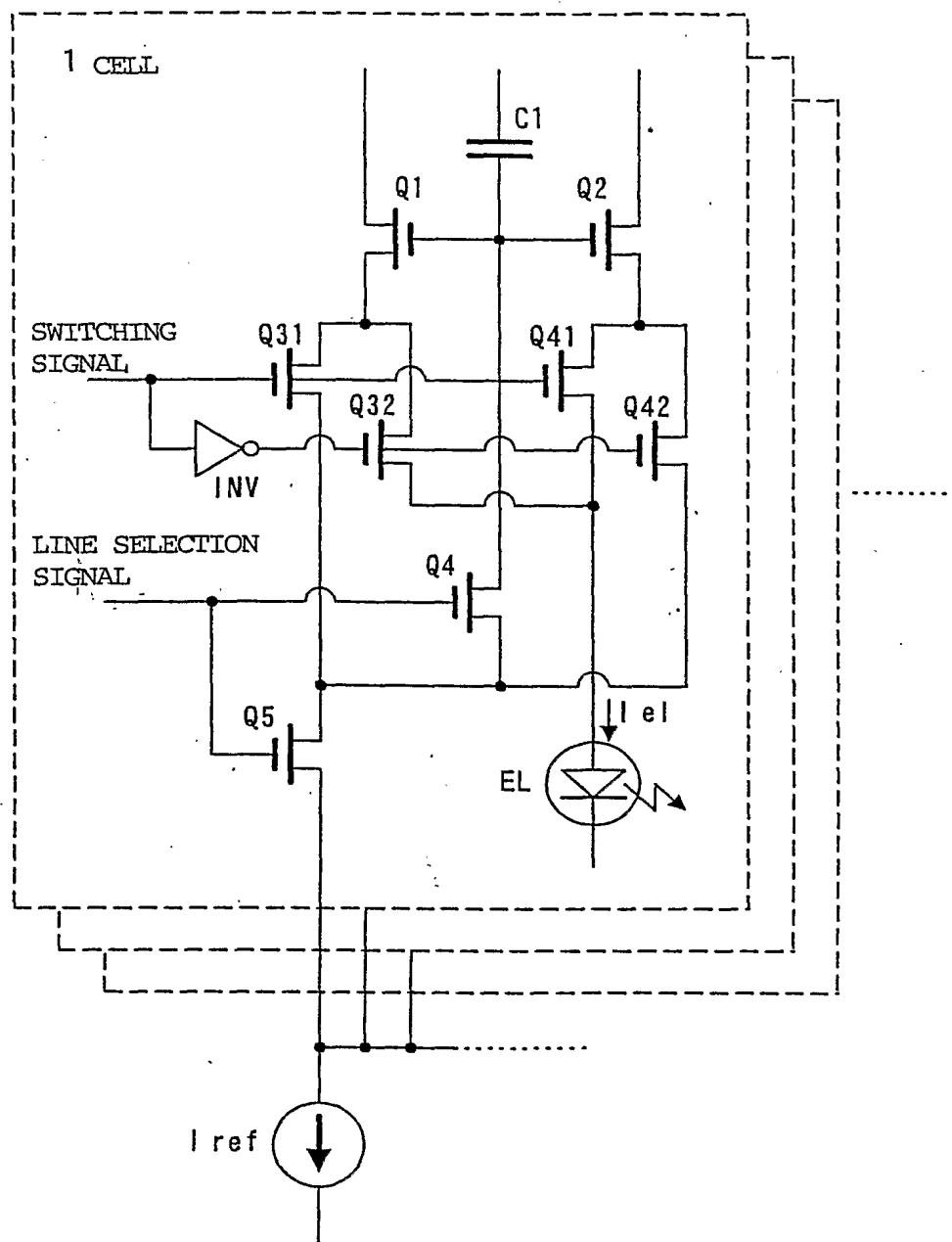


FIG. 8

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
24 April 2003 (24.04.2003)

PCT

(10) International Publication Number
WO 03/034381 A3

(51) International Patent Classification⁷: **G09G 3/32, 3/36**

[JP/JP]; c/o Corporate Research and Development Laboratory, Pioneer Corporation, 6-1-1, Fujimi, Tsurugashima-shi, Saitama 350-2288 (JP).

(21) International Application Number: PCT/JP02/09265

(74) Agent: **FUJIMURA, Motohiko**; Fujimura & Associates, Ginza-Ohno Bldg., 1-17, Tsukiji 4-chome, Chuo-ku, Tokyo 104-0045 (JP).

(22) International Filing Date:
11 September 2002 (11.09.2002)

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(25) Filing Language: English

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,

(26) Publication Language: English

(30) Priority Data:
2001-286064 20 September 2001 (20.09.2001) JP

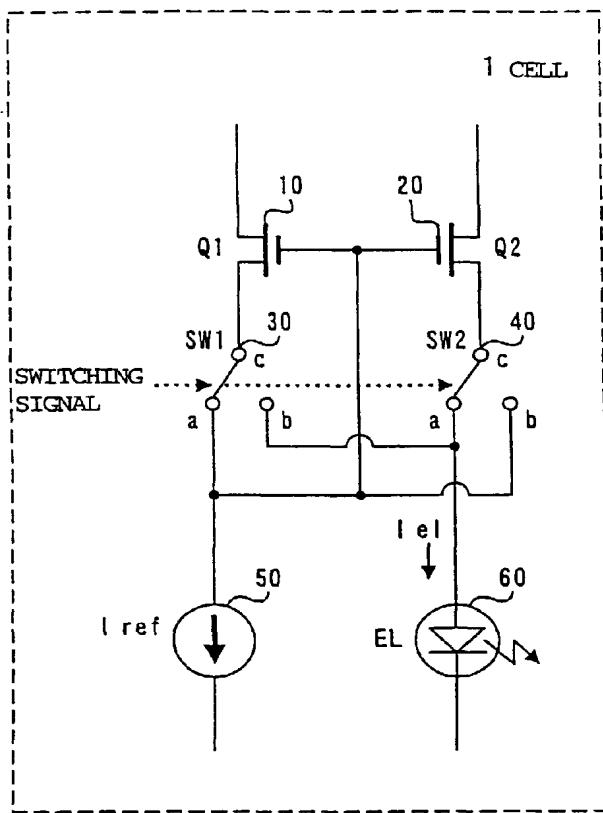
(71) Applicant (for all designated States except US): **PIioneer CORPORATION** [JP/JP]; 4-1, Meguro 1-chome, Meguro-ku, Tokyo 153-8654 (JP).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **OKUDA, Yoshiyuki**

[Continued on next page]

(54) Title: DRIVE CIRCUIT FOR LIGHT EMITTING ELEMENTS



(57) Abstract: A display panel includes a number of light emitting cells arranged in a matrix. At least one drive circuit is associated with the light emitting cells. Each cell includes one light emitting element. A current mirror circuit is used in the drive circuit. The current mirror circuit has a primary transistor to drive a reference current source and a secondary transistor to drive the light emitting element. A pulse signal selects one of the primary and secondary transistors alternately. This switching operation by the pulse signal reduces irregularities in mirror ratio between the two transistors in each light emitting cell. As a result, the drive circuit(s) can suppress fluctuations in brightness among the light emitting cells of the display panel.

WO 03/034381 A3



ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(88) Date of publication of the international search report:
27 November 2003

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International Application No

PCT/JP 02/09265

A. CLASSIFICATION OF SUBJECT MATTER
 IPC 7 G09G3/32 G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

PAJ, WPI Data, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 99 65011 A (KONINKL PHILIPS ELECTRONICS NV ;PHILIPS SVENSKA AB (SE)) 16 December 1999 (1999-12-16) abstract the whole document ----	1-20
A	EP 1 132 882 A (LG ELECTRONICS INC) 12 September 2001 (2001-09-12) abstract paragraph '0073! – paragraph '0080!; claim 1; figure 4 ----	1,10,18
E	US 2003/020705 A1 (NAKAMURA HIROYUKI ET AL) 30 January 2003 (2003-01-30) abstract paragraph '0104! – paragraph '0108!; claims 1-11; figure 5 -----	1-20



.Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

° Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
- "L" document which may throw doubts on priority, claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

12 September 2003

Date of mailing of the international search report

22/09/2003

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL – 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Wolff, L

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/JP 02/09265

Patent document cited in search report		Publication date		Patent family member(s)		Publication date
WO 9965011	A	16-12-1999	EP WO JP US	1034530 A2 9965011 A2 2002517806 T 6373454 B1		13-09-2000 16-12-1999 18-06-2002 16-04-2002
EP 1132882	A	12-09-2001	KR CN EP US	2001087002 A 1312535 A 1132882 A2 2001019327 A1		15-09-2001 12-09-2001 12-09-2001 06-09-2001
US 2003020705	A1	30-01-2003	WO WO US	02075710 A1 02077958 A1 2003016191 A1		26-09-2002 03-10-2002 23-01-2003